Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claims 1 and 2 (Canceled)

Claim 3 (Currently Amended): [[The]] A semiconductor device which is provided with a temperature detection circuit for measuring a temperature of a CPU using a temperature dependency of off leak currents of transistors and which is provided in a chip on which the CPU is mounted ~~according to Claim 2~~, wherein the temperature detection circuit comprises:

a temperature detection part for increasing a potential of a live node connected to a stray capacitance by charging the stray capacitance of the transistors with the off leak currents, and for detecting that a temperature of the CPU reaches a given temperature by comparing a potential level of the live node with a threshold value of [[the]] a transistor, and

a detection signal output part for outputting and holding a detection signal which is driven by a signal issued by the temperature detection part.

Claim 4 (Original): The semiconductor device according to Claim 3, wherein the

temperature detection part comprises a first PMOS transistor and a first NMOS transistor connected in series between a power supply potential VDD and a grounding potential, and the live node is a junction between a drain of the first PMOS transistor and a drain of the first NMOS transistor, and the stray capacitance between the live node and the grounding potential is charged with a current differential between the off leak current of the first PMOS transistor and the off leak current of the first NMOS transistor when the first PMOS transistor and the first NMOS transistor are in OFF state.

Claim 5 (Currently Amended): The semiconductor device according to Claim 4 [[3]], wherein the detection signal output part comprises:

a second PMOS transistor connected between the power supply potential VDD and the grounding potential,

a series circuit comprised of second and third NMOS transistors connected in series to each other, and

a data holding circuit connected to an output node of the series circuit,

wherein a drain of the second PMOS transistor is connected to the output node and a drain of the second NMOS transistor, [[while]] a gate of the second NMOS transistor is connected to a gate of the first PMOS transistor, ~~and a drain thereof~~ a source of the second NMOS transistor is connected to a drain of the third NMOS transistor, [[and]] a gate of the third NMOS transistor is connected to the live node, and a source of the third NMOS transistor ~~thereof~~ is grounded, and

wherein the output node is pre-charged by the second PMOS transistor when starting [[the]] detection of the temperature, and the second and third NMOS transistors are rendered in an ON state when a potential of the live node exceeds a threshold value of the third NMOS transistor, so that [[the]] a pre-charged electric charge accumulated in the output node is discharged to change [[the]] a potential of the output node [[and]], whereby the changed potential is [[hkept]] held in the data holding circuit.

Claim 6 (Currently Amended): The semiconductor device according to Claim 5, wherein the detection signal output part further comprises a third PMOS transistor having a source connected to the power supply potential VDD ~~at its source~~, a gate connected to the output node ~~at its gate~~, and a drain connected to the live node ~~at its drain~~, [[and]]

wherein said third PMOS transistor is rendered in the ON state when the temperature of the CPU reaches a set temperature, [[and]] so that the pre-charged electric charge of the output node is discharged to accelerate the charging of the stray capacitance of the live node.

Claim 7 (New): A detection circuit that detects a temperature of a CPU, the detection circuit and the CPU being mounted on a same chip, the detection circuit comprising:

a precharge circuit that precharges an output node;

a transistor pair that charge a stray capacitance at a live node with off leak

current that is temperature dependent; and

a switch, coupled between the output node and ground, that discharges the output node responsive to a potential at the live node, so that a potential of the output node is indicative that the CPU exceeds a predetermined temperature.

Claim 8 (New): The detection circuit of claim 7, wherein said transistor pair comprises a first PMOS transistor and a first NMOS transistor coupled together in series between a power supply potential and ground, wherein the live node is a junction between a drain of the PMOS transistor and a drain of the NMOS transistor.

Claim 9 (New): The detection circuit of claim 8, wherein said switch comprises second and third NMOS transistors coupled together in series between the output node and ground, wherein the third NMOS transistor is responsive to the potential at the live node.

Claim 10 (New): The detection circuit of claim 9, wherein the second NMOS transistor has a gate coupled to a gate of the first PMOS transistor, a drain coupled to the output node, and a source, and

the third NMOS transistor has a gate coupled to the live node, a drain coupled to the source of the second NMOS transistor, and a source coupled to ground.

Claim 11 (New): The detection circuit of claim 8, further comprising a second PMOS transistor having a gate coupled to the output node, a source coupled to the power supply potential and a drain coupled to the live node.

Claim 12 (New): The detection circuit of claim 8, wherein said precharge circuit comprises a second PMOS transistor having a gate coupled to a precharge control signal, a source coupled to the power supply potential and a drain coupled to the output node.

Claim 13 (New): The detection circuit of claim 7, further comprising a holding circuit that holds the potential of the output node.